

PATENT ABSTRACTS OF JAPAN

(11)Publication number : **04-127601**
 (43)Date of publication of application : **28.04.1992**

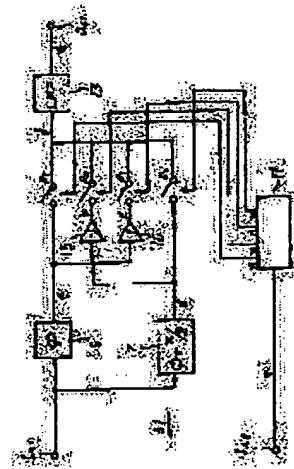
(51)Int.CI.

H03D 7/00

(21)Application number : **02-247957**(71)Applicant : **VICTOR CO OF JAPAN LTD**(22)Date of filing : **18.09.1990**(72)Inventor : **ISHIGAKI YUKINOBU****(54) FREQUENCY CONVERSION CIRCUIT****(57)Abstract:**

PURPOSE: To eliminate the need for provision of DC balance by applying \leq sets of timing pulse to \leq sets of switches, applying switching control to each switch so as to output a signal whose frequency is converted into a sum or a difference between an input signal frequency and a local oscillating signal frequency from a low pass filter.

CONSTITUTION: A clock signal (e) is fed to a timing pulse generator 11 from an input terminal I_{12} and the timing pulse generator 11 generates an outputs timing pulses T1-T4 and they are fed to switches S1-S4 respectively, which are on/off-controlled. That is, when each of the timing pulses T1-T4 is at an H level, since the switches S1-S4 are closed, signals (j) are synthesized and the resulting signal is fed to an LPF (low pass filter) 13. A high frequency switching component is eliminated in the LPF 13 and a signal (k) is outputted from an output terminal Out. Thus, a problem of DC balance or linearity or the like is not almost caused.

**LEGAL STATUS**

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office